Intelligent Systems

Industry Standard Architecture (ISA) Support on the Intel® Atom™ Processor E3800 Product Family & Intel® Celeron® Processor N2807/N2930/J1900 Platform

IOTG Platform Application Engineering

Revision 1.6

Document Number: 517493

Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to: http://www.intel.com/design/literature.htm

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families: Go to: Learn About Intel® Processor Numbers

Celeron, Intel, the Intel logo, Intel Atom, are trademarks of Intel Corporation in the U.S. and/or other countries

*Other names and brands may be claimed as the property of others.

Revision History

Date	Revision	Description
February 2013	1.0	Initial Release
August 2013	1.1	Added information regarding 'PCI Legacy Mode'
September 2013	1.2	Page 6 • Correct the first Note paragraph • Add definition for PCI Legacy Mode
September 2013	1.3	• Delete or update Bay Trail name to marketing version • Removed slide 11
December 2013	1.4	• Correct marketing naming • Update Reference Documents
December 2013	1.5	• Update Disclaimer page
July 2014	1.6	• Update product naming

Overview

- ISA (Industry Standard Architecture) bus support is still a requirement for some Intelligent System vendors

- This document is intended to indicate important considerations when implementing ISA support

- The information in this document is presented as deltas to the following White Paper: *Implementing Industry Standard Architecture (ISA) with Intel® Express Chipsets*

ISA Bridge Support and Limitations

- **PCI / ISA Bridge**
  - As described in White Paper #318244 plus
    - The SoC does not natively support PCI. A PCI Express* to PCI bridge is required to implement PCI.

      The following list of bridge vendors is provided only as an example of providers of the type of component that could be used to implement PCI support on the Intel® Atom™ Processor E3800 Product Family & Intel® Celeron® Processor N2807/N2930/J1900 platform. The specific vendors named are not intended to be a recommendation of any kind nor any guarantee of suitability.

      - IDT*
      - Marvell*
      - Pericom*
      - PLX Technology*
      - Texas Instruments*

ISA Bridge Support and Limitations

- **PCI / ISA Bridge**
  - As described in White Paper #318244 plus
    - The SoC does not natively support PCI. A PCI Express* to PCI bridge is required to implement PCI.

    - **Note:** The SoC does not support the configuration of any of its PCI Express* root ports as a subtractive decode agent. The iLB (Intel Legacy Block) is the only supported agent.

      As such, the SoC does not support 'PCI Legacy Mode' since it is not possible to configure the PCI Express* root port to subtractively decode and forward legacy cycles downstream

      PCI Legacy Mode is defined as the PCI Express root port having the capability to subtractively decode and forward legacy cycles to a PCIe-to-PCI bridge, and the bridge continues forwarding legacy cycles to downstream PCI devices

ISA Bridge Support and Limitations

- **LPC / ISA Bridge**
  - Memory Transactions: The SoC does support memory mapped transactions on the LPC bus.

    Note: See the Intel® Pentium® Processor N3500-series, J2850, J2900, and Intel® Celeron® Processor N2900-series, N2800-series, J1800-series, J1900, J1750 External Design Specification (EDS) and Intel® Atom™ Processor E3800 Product Family Datasheet for further details

  - Other Limitations: As described in White Paper #318244 plus
    - The SoC does not implement the optional LDRQ# LPC signal. As such DMA/Bus Mastering support is not available to the LPC/ISA bridge.

Architectural Limitations

- **IO Aliasing:**
  - As described in White Paper #318244 plus
    - The SoC does not implement the ISA Enable (IE) bit. As such automatic compensation for I/O address aliasing is not available.

- **Plug and Play:**
  - As described in White Paper #318244

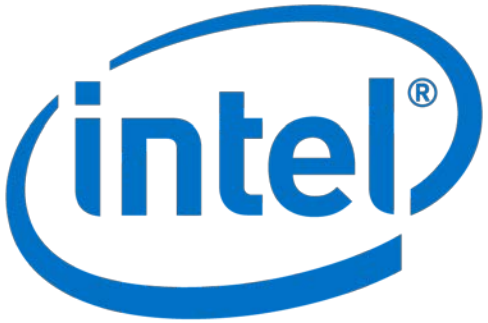
Backup

Reference Documents

- Implementing Industry Standard Architecture (ISA) with Intel® Express Chipsets (intel.com: #318244)
- Intel® Pentium® Processor Intel® Pentium® Processor N3500-series, J2850, J2900, and Intel® Celeron® Processor N2900-series, N2800-series, J1800-series, J1900, J1750 External Design Specification (EDS) (IBP #512177)
- Intel® Atom™ Processor E3800 Product Family Datasheet (IBP #538136)

Terminology

- DMA: Direct Memory Access
- I/O: Input/Output
- ISA: Industry Standard Architecture
- LPC: Low Pin Count
- PCI: Peripheral Component Interconnect
- SoC: The Intel® Atom™ Processor E3800 Product Family & Intel® Celeron® Processor N2807/N2930/J1900



Intelligent Systems